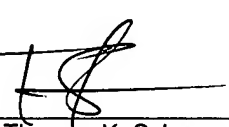




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| TRANSMITTAL OF APPEAL BRIEF  |  |                                  | Docket No.<br>03226/157001; P6865 |                            |
|--|--|----------------------------------|-----------------------------------|----------------------------|
| In re Application of: Sudhakar Bobba et al.  |  |                                  |                                   |                            |
| Application No.<br>10/033,008-Conf. #7852  |  | Filing Date<br>December 28, 2001 |                                   | Examiner<br>D. E. Graybill |
|  |  |                                  |                                   | Group Art Unit<br>2822     |
| Invention: CURRENT CROWDING REDUCTION TECHNIQUE USING SLOTS  |  |                                  |                                   |                            |
| <b><u>TO THE COMMISSIONER OF PATENTS:</u></b>  |  |                                  |                                   |                            |
| Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: <u>November 7, 2005</u> .  |  |                                  |                                   |                            |
| The fee for filing this Appeal Brief is _____.   |  |                                  |                                   |                            |
| <input type="checkbox"/> Large Entity <input type="checkbox"/> Small Entity  |  |                                  |                                   |                            |
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| <input type="checkbox"/> A check in the amount of _____ is enclosed.   |  |                                  |                                   |                            |
| <input type="checkbox"/> Charge the amount of the fee to Deposit Account No. <u>50-0591</u> .<br>This sheet is submitted in duplicate.   |  |                                  |                                   |                            |
| <input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.  |  |                                  |                                   |                            |
| <input checked="" type="checkbox"/> The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. <u>50-0591</u> .<br>This sheet is submitted in duplicate.            |  |                                  |                                   |                            |
| <br>_____<br>Thomas K. Scherer<br>Attorney Reg. No. : 45,079<br>OSHA · LIANG LLP<br>1221 McKinney St., Suite 2800<br>Houston, Texas 77010<br>(713) 228-8600 |  |                                  | Dated: <u>June 28, 2007</u>       |                            |



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**I. REAL PARTY IN INTEREST**

The real party in interest in the present application is Sun Microsystems, Inc., assignee of all rights and interests in the present application. Assignment to Sun Microsystems, Inc. from the inventors, Sudhakar Bobba and Tyler Thorp, was recorded in the United States Patent and Trademark Office on December 28, 2001 at Reel 012423, Frame 0768.

**II. RELATED APPEALS AND INTERFERENCES**

To the best knowledge of the Appellant and the Appellant's legal representative, there are no other appeals or interferences that will directly affect, be affected by, or have a bearing on the decision of the Board in the pending appeal.

**III. STATUS OF CLAIMS**

Claims 1 – 18 were pending in the present application. By way of the Response to the Restriction Requirement of June 29, 2004, claims 15 – 18 were withdrawn from consideration. Accordingly, claims 1 – 14 are currently pending in the present application.

Claims 1 – 14 were rejected in the final Office Action of March 4, 2005. *See* final Office Action of March 4, 2005, Office Action Summary (page 1). Specifically, claims 1 – 14 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,689,139 (hereinafter “Bui”). *See id.* at pages 2 – 3. Claims 1 – 14 were further rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter “AAPA”) and Bui. *See id.* at pages 3 – 5.

The rejections of claims 1 – 14 are hereby appealed.

#### IV. STATUS OF AMENDMENTS

No amendments have been made during the prosecution of the present application. The claims of record in the present application are presented in Section IX, *infra*.

#### V. SUMMARY OF CLAIMED SUBJECT MATTER

##### A. *Prior Art*

Referring to Figure 4a of the present application, an integrated circuit (40) is formed of a plurality of metal layers M1 – M8. *See* Specification, paragraph [0004]. As further described in the Specification:

The metal layers, M1-M8, are connected to each other by conductive pathways (50) known as “vias.” Vias (50) are essentially holes within the dielectric material (48) that have been doped with metal ions. . . . Signals that need to be transmitted/received to/from the metal layers, M1-M8, and vias (50) to the top metal layer, M8. The top metal layer, M8, then transmits/receives signal and power to/from the bumps (44) located on the active side of the integrated circuit (40).

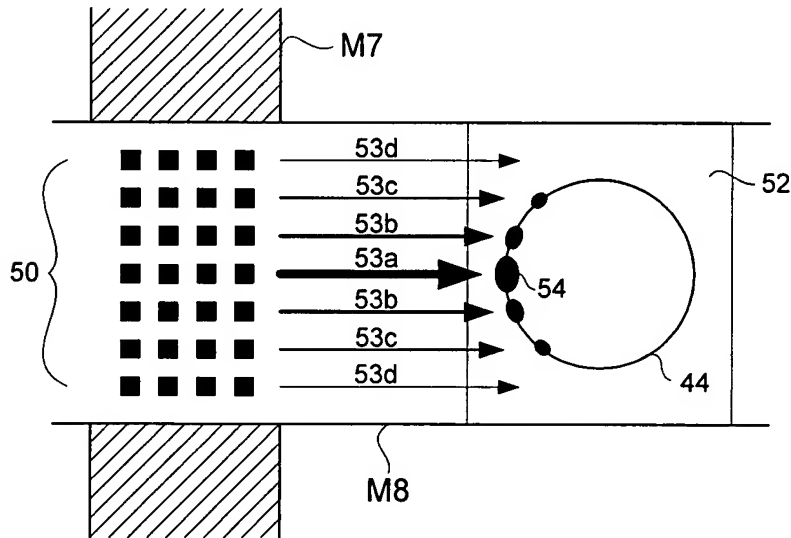
*See id.* at paragraphs [0004] – [0005].

Figure 4c of the present application (reproduced below) shows a top view of a top metal layer, M8, of an integrated circuit. *See id.* at paragraph [0024]. The top metal layer, M8, propagates current between vias (50) and bump (44). *See id.* at paragraph [0025]. As further described in the Specification:

Although the vias (50) facilitate current flow, because the vias (50) are positioned laterally across the layer M8, and the bump (44) is circular, there is non-uniform current density at the junction between the bump (44) and the top metal layer, M8. This non-uniform current density, resulting

from the differences in current path length from the vias (50) to the bump (44), is known as “current crowding.” In this current crowding phenomenon, there is high current density at a region (54) of the bump (44) that is in closest proximity to the vias (50), and there is lower current density in the rest of the junction between the bump (44) and the landing pad (52).

*See id.*



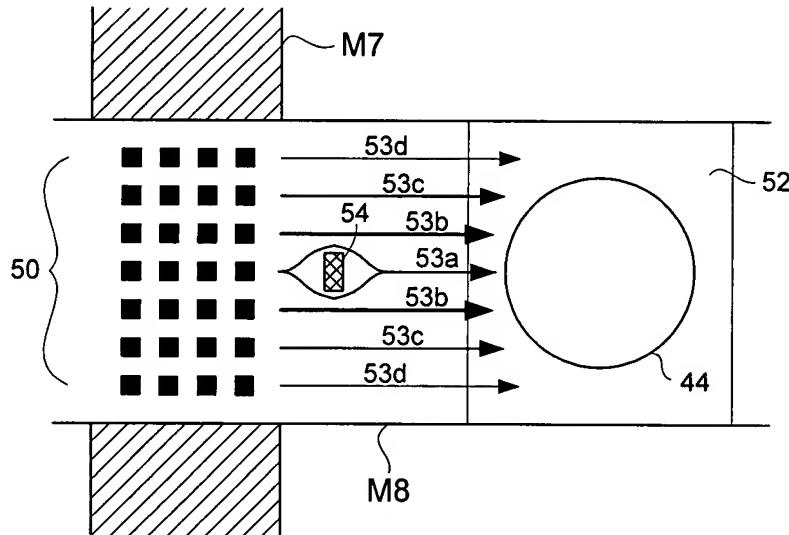
**FIGURE 4c**  
**(Prior Art)**

Such current crowding is undesirable because prolonged exposure to current crowding may cause, among other things, performance degradation, power distribution deficiencies, signal delay, and damage to the junction between the bump (44) and landing pad (52). In some cases, damage caused by electro-migration may actually result in detachment of the bump. *See id.* at paragraph [0026].

***B. Claimed Invention***

Referring to, for example, Figure 5a of the present application (reproduced below), in order to reduce or mitigate the existence or effects of current crowding, embodiments of the claimed invention have at least one slot (54) formed in the top metal

layer, M8, the slot (54) having the effect of lengthening the current path length from vias (50) in a central region of the top metal layer, M8, to bump (44). *See id.* at paragraph [0027]. Such an effect results in the reduction of current crowding at bump (44). *See id.*



**FIGURE 5a**

Independent claim 1 reads:

A bump and via structure, comprising:  
a metal layer;  
a plurality of vias connecting the metal layer to another metal layer;  
a bump mounted on the metal layer; and  
a first slot formed in the metal layer between the vias and the bump.

Independent claim 8 reads:

An integrated circuit, comprising:  
a metal layer;  
a plurality of vias connecting the metal layer to another metal layer;  
a bump mounted on the metal layer; and  
a first slot formed in the metal layer between the vias and the bump.

Thus, independent claims 1 and 8 of the present application each require (i) a metal layer (M8), (ii) a plurality of vias (50) connecting the metal layer (M8) to another

metal layer (M7), (iii) a bump (44) mounted on the metal layer (M8), and (iv) a slot (54) formed in the metal layer (M8) between the vias (50) and the bump (44).

## **VI. GROUNDS OF REJECTION**

The grounds of rejection presented for review are as follows:

- 1) whether Bui anticipates claims 1 – 14 under 35 U.S.C. § 102(b); and
- 2) whether Bui and AAPA render claims 1 – 14 unpatentable under 35 U.S.C. § 103(a).

## **VII. ARGUMENT**

### *A. Bui Fails to Anticipate Claims 1 – 14 Under 35 U.S.C. § 102(b)*

Bui recognizes that “semiconductor devices comprise[] . . . a plurality of levels with conductive patterns in electrical contact by means of conductive vias and interconnection lines.” *See* Bui, column 7, lines 17 – 20. As shown in Figure 3 of Bui, a first metal interconnection line **30** is in electrical contact with vias **32A** and **32B**, and a second metal interconnection line **31** is in electrical contact with vias **32B** and **32C**. *See id.* at column 9, lines 27 – 33. The metal interconnection lines **30, 31** are provided with slots **33** that are formed through the metal interconnection lines **30, 31** so that the total width of metal across the interconnection lines **30, 31** is selected for optimum electromigration lifetime in accordance with the Bamboo effect for that metal. *See id.* at column 9, lines 33 – 38; Abstract. Thus, Bui discloses metal interconnection lines that are in contact with vias and that have slots formed therein.



In the final Office Action of March 4, 2005, the Examiner relied on Figure 5 of Bui and the description thereof as disclosing those limitations of the claimed invention requiring a bump. However, Bui's disclosure is completely silent as to a bump and instead clearly discloses filling a via:

. . . the Backflow Potential Capacity is further optimized by employing a material to fill the conductive via different from the metal of the interconnection line. Thus, when employing an aluminum or aluminum alloy metal interconnection line 50, as shown in FIG. 5, it is preferred to employ a tungsten plug filling the via 51 through insulating layers 52, or a plug comprising aluminum or aluminum alloy 43 with a barrier layer 54 and/or anti-reflection coating 55.

See Bui, column 7, lines 54 – 63 (emphasis added).

Despite repeated assertions by Applicant that bumps are technically distinct from vias,<sup>1</sup> the Examiner has continued to maintain that Figure 5 of Bui discloses a bump, even

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<sup>1</sup> See, e.g., Response to Office Action of October 6, 2004, page 3 (“The Examiner’s characterization of element 53 in Figure 5 of Bui as a ‘bump’ is incorrect in that element 53 is a plug ‘filling the via 51 through insulating layers 52.’ See Bui, column 7, lines 57 – 61. Those skilled in the art will clearly note that the conductive material used to fill a via is entirely distinct from an electrical bump formed on a metal layer.”); Response to final Office Action of March 4, 2005, page 2 (“The Examiner asserts Bui’s element 53 in Figure 5 . . . is a bump because it is a ‘relatively abrupt protuberance on a surface.’ See final Office Action dated March 4, 2005 at page 2 and page 3. Bui’s Figure 5 illustrates insulating layers (element 52) surrounding a via (element 51). Bui’s via (element 51) is a tunnel cutting vertically through the otherwise solid insulating layers (element 52). Bui discloses filling the via (element 51) with a tungsten plug or a plug comprising aluminum (element 53; column 7, lines 57-63). Applicant respectfully asserts the plug (element 53)

though Bui itself describes Figure 5 as showing a via. As clear to one of ordinary skill in the art and as described in the present application, vias connect metal layers within a integrated circuit (*see* vias (50) in Figure 4a of the present application), whereas bumps are conductive deposits on a top metal layer of an integrated circuit (*see* bumps (44) in Figure 4a of the present application) that are used to transmit/receive signals external to the integrated circuit. *See* Section V, *supra*. Simply stated, the via 51 shown in Figure 5 of Bui *is not* a bump.

As Bui is completely silent as to a bump, Bui necessarily cannot and does not disclose a metal layer having a slot formed between vias and a bump mounted on the metal layer as required by independent claims 1 and 8 of the present application. Accordingly, independent claims 1 and 8 are patentable over Bui. Dependent claims 2 – 7 and 9 – 13 are patentable for at least the same reasons.

*B. Bui and AAPA Fail to Render Claims 1 – 14 Obvious Under 35 U.S.C. § 103(a)*

In order to render claims 1 – 14 obvious under 35 U.S.C. § 103(a), Bui and AAPA must disclose each and every element of the claimed invention. *See In re Royka*, 490 F.2d 981 (C.C.P.A. 1974); MPEP § 2143.03. As discussed above, Bui fails to at least disclose a metal layer having a slot formed between vias and a bump mounted on the metal layer as required by independent claims 1 and 8 of the present application. As to AAPA, AAPA is completely silent as to slots formed between vias and a bump mounted on a metal layer. Thus, AAPA clearly fails to disclose those limitations of the claimed

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disclosed in Bui is not equivalent to the bump recited in the claims of the present invention.”).

invention not disclosed in Bui. Accordingly, independent claims 1 and 8 are patentable over Bui and AAPA, whether considered separately or in combination. Dependent claims 2 – 13 and 9 – 13 are patentable for at least the same reasons.

Moreover, in order to render claims 1 – 14 obvious under 35 U.S.C. § 103(a), Bui and AAPA must be properly combinable in view of the law applicable to § 103. *See* MPEP § 2143. The Examiner cannot combine prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. Instead, there must a suggestion or motivation to combine the references within the prior art references themselves. In other words, regardless of whether prior art references can be combined, there must an indication within the prior art references *expressing desirability* to combine the references. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990) (emphasis added). Further, the present application *cannot be used a guide* in reconstructing elements of prior art references to render the claimed invention obvious. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (emphasis added).

Bui is directed to a technique for improving the electromigration lifetime of a metal interconnection line. *See* Bui, Abstract. This technique involves the use of slots in a metal interconnection line so that the total width of metal across the metal interconnection line is selected for optimum electromigration lifetime in accordance with the Bamboo effect for that metal. *See id.* On the other hand, AAPA describes the existence of current crowding (*i.e.*, non-uniform current density) at particular regions of a bump mounted on a metal layer. *See* Specification, paragraph [0025]. In the final Office Action of March 4, 2005, the Examiner stated that “it would have been obvious to combine this disclosure of Bui with the disclosure of [AAPA] because it would enhance

the electromigration lifetime of the metal layer.” *See* final Office Action of March 4, 2005, page 5. However, AAPA is not at all concerned with the electromigration lifetime of metal layers; instead, AAPA describes current crowding at particular regions of a bump. *See* Specification, paragraph [0025]. Conversely, Bui, which is completely silent as to a bump, is necessarily not at all concerned with current crowding at particular regions of a bump. *See* Section VII, Part A, *supra*. Thus, there is clearly no expression of desirability within either Bui or AAPA to motivate one skilled in the art to turn to the teachings of the other. As set forth above, regardless of whether a group of references discloses all the limitations of a claimed invention, there must be an expression of desirability within the references to combine the references. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). Such an expression is clearly lacking in Bui and AAPA. Thus, the combination of Bui and AAPA in a § 103 rejection of any of the claims of the present application is improper.

Accordingly, Bui and AAPA (i) are not properly combinable under § 103 in the instant case, and (ii) whether considered separately or in combination, fail to disclose each and every element of claims 1 – 14.

### XIII. CONCLUSION

The Summary of Claimed Subject Matter provided in Section V, *supra*, in combination with the arguments presented in Section VII, *supra*, clearly show that claims 1 – 14 of the present application are patentable over the prior art of record. Therefore, Appellant respectfully requests that the Board reverse the Examiner's rejections of claims 1 – 14.

Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference No. 03226.157001; P6865).

Respectfully submitted,

Date: 6/28/07



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**IX. CLAIMS APPENDIX**

1. A bump and vias structure, comprising:
  - a metal layer;
  - a plurality of vias connecting the metal layer to another metal layer;
  - a bump mounted on the metal layer; and
  - a first slot formed in the metal layer between the vias and the bump.
2. The bump and vias structure of claim 1, wherein the bump is mounted on the metal layer via a landing pad.
3. The bump and vias structure of claim 1, further comprising second and third slots disposed between the first slot and the bump.
4. The bump and vias structure of claim 3, wherein the second and third slots are displaced laterally along the metal layer and form an aperture therebetween that is centered with respect to the first slot.
5. The bump and vias structure of claim 1, wherein the first slot comprises a section of the metal layer that is evacuated of conductive material.
6. The bump and vias structure of claim 1, wherein the first slot comprises a current-resistant material.

7. The bump and vias structure of claim 1, wherein the first slot comprises a dielectric material.
8. An integrated circuit, comprising:
  - a metal layer;
  - a plurality of vias connecting the metal layer to another metal layer;
  - a bump mounted on the metal layer; and
  - a first slot formed in the metal layer between the vias and the bump.
9. The integrated circuit of claim 8, wherein the bump is mounted on the metal layer via a landing pad.
10. The integrated circuit of claim 8, further comprising second and third slots disposed between the first slot and the bump.
11. The integrated circuit of claim 10, wherein the second and third slots are displaced laterally along the metal layer and form an aperture therebetween that is centered with respect to the first slot.
12. The integrated circuit of claim 8, wherein the first slot comprises a section of the metal layer that is evacuated of conductive material.

13. The integrated circuit of claim 8, wherein the first slot comprises a current-resistant material.
14. The integrated circuit of claim 8, wherein the first slot comprises a dielectric material.
- 15-18. (Withdrawn)



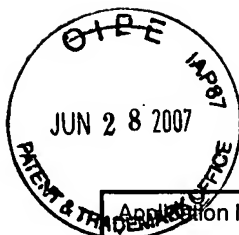
**X. EVIDENCE APPENDIX**

No evidence of the types described in 37 CFR § 41.37(c)(1)(ix) has been submitted during prosecution of the present application.

**XI. RELATED PROCEEDINGS APPENDIX**

As indicated in Section II *supra*, to the best knowledge of Appellant and the Appellant's legal representative, there are no decisions rendered by a court or the Board that may directly affect, be affected by, or have a bearing on the decision of the Board in the pending appeal.

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Application No. (if known): 10/033,008

Attorney Docket No.: 03226/157001; P6865

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